

What is claimed is:

1 1. A ball grid array package, comprising:  
2 a substrate which has a top surface and an opposite  
3 bottom surface, said bottom surface having an outer array of  
4 contact pads each separated from each other by a first  
5 distance, and a center array of contact pads each separated  
6 from each other by a second distance, said center array of  
7 contact pads being separated from said outer array of  
8 contact pads by a third distance which is larger than the  
9 first and second distances; and,  
10 a plurality of solder balls attached to said contact  
11 pads of said substrate.

1 2. The package as recited in claim 1, wherein said top  
2 surface of said substrate has a plurality of bond pads.

1 3. The package as recited in claim 2, wherein said top  
2 surface of said substrate has a ground bus that is connected  
3 to said center array of contact pads by a plurality of vias  
4 that extend through said substrate.

1 4. The package as recited in claim 3, wherein said  
2 outer array of contact pads has at least five rows of  
3 contact pads.

1           5. The package as recited in claim 4, wherein said top  
2 surface of said substrate has a power bus that is connected  
3 to said center array of contact pads by a plurality of vias  
4 that extend through said substrate.

1           6. The package as recited in claim 5, wherein said  
2 center array of contact pads is arranged in a four by four  
3 matrix.

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1           7. A ball grid array integrated circuit package,  
2 comprising:

3           a substrate which has a top surface and an opposite  
4 bottom surface, said top surface having a plurality of bond  
5 pads, said bottom surface having an outer array of contact  
6 pads each separated from each other by a first distance, and  
7 a center array of contact pads each separated from each  
8 other by a second distance, said center array of contact  
9 pads being separated from said outer array of contact pads  
10 by a third distance which is larger than the first and  
11 second distances;

12           a plurality of solder balls attached to said contact  
13 pads of said substrate; and,

14           an integrated circuit that is mounted to said substrate  
15 and coupled to said bond pads.

1        8. The package as recited in claim 7, wherein said top  
2 surface of said substrate has a ground bus that is coupled  
3 to said integrated circuit and connected to said center  
4 array of contact pads by a plurality of vias that extend  
5 through said substrate.

1        9. The package as recited in claim 8, wherein said  
2 outer array of contact pads has at least five rows of  
3 contact pads.

1        10. The package as recited in claim 9, wherein said  
2 top surface of said substrate has a power bus that is  
3 connected to said center array of contact pads by a  
4 plurality of vias that extend through said substrate.

1        11. The package as recited in claim 10, wherein said  
2 center array of contact pads is arranged in a four by four  
3 matrix.

1        12. The package as recited in claim 11, wherein said  
2 integrated circuit is enclosed by an encapsulant.

1        13. The package as recited in claim 7, wherein said  
2 outer array of contact pads is located outside an outer  
3 dimensional profile of said integrated circuit.

1 14. A method for assembling a ball grid array  
2 integrated circuit package, comprising the steps of:  
3 a) providing a substrate which has a top surface and  
4 an opposite bottom surface, said bottom surface having an  
5 outer array of contact pads each separated from each other  
6 by a first distance, and a center array of contact pads each  
7 separated from each other by a second distance, said center  
8 array of contact pads being separated from said outer array  
9 of contact pads by a third distance which is larger than the  
10 first and second distances;  
11 b) mounting an integrated circuit to said top surface  
12 of said substrate; and,  
13 c) attaching a plurality of said solder balls to said  
14 contact pads.

1 15. The method as recited in claim 14, further  
2 comprising the step of encapsulating said integrated  
3 circuit.

1 16. The method as recited in claim 15, further  
2 comprising the step of coupling said integrated circuit to  
3 said substrate with a plurality of bond wires.

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